FiPS and M2DC: Novel Architectures for Reconfigurable Hyperscale Servers

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Rising demand for computing power
- Complexity of calculations
- Increasing number of users

Energy consumption is rising
- 15% of electrical energy consumption by computers
- CO₂ emissions

Systems have to be cooled
- Complexity/Cost rising

→ Integrate FPGA / ARM
→ Founded by EC
Developing Hardware and Design Methodologies for Heterogeneous Low Power Field Programmable Servers
FiPS Achievements

• Modular heterogeneous server system and middleware
  • Up to 72 microservers in a single 1 RU server
  • Supports x86/ARM CPUs, GPGPUs, and FPGAs
  • OpenCL runtime for FPGA modules
Apalis-based microservers

- Microservers based on ARM-SoCs ranging from Cortex-A9 to Cortex-A15
- Xilinx Zynq-based microserver

COM Express-based microservers

- x86 microservers ranging from Atom single cores to i7 quad core
- FPGA-based COM Express microserver, integrating Xilinx Zynq SoC
• Zynq 7045, ARM Cortex A9 Dual Core, 1 GHz
• Tightly integrated Programmable Logic
• Memory interfaces
  • 1 GByte DDR3 (32-bit) PS Memory
  • Up to 8 GByte DDR3 SO-DIMM module (64-bit-wide) PL Memory
  • eMMC memory (16 GByte)
  • Secure Digital (SD) card slot
• All COM Express interfaces
  • PCIe, Gigabit Ethernet, USB, DP, SATA, CAN, …
• High-Speed Serial Links (dedicated connector)
  • Up to 8 lanes, 12.5 Gbit/s each
  • Crosspoint switch for network reconfiguration
• Expansion piggyback (e.g. for I/O, Accelerators)
• Zynq 7020, ARM Cortex A9 Dual Core, 866 MHz
• Memory
  • 1 GByte of DDR3 (32-bit) PS Memory
  • eMMC memory (16 GByte)
  • Secure Digital (SD) card slot
• Apalis Module Interface
  • Compatible with Toradex Apalis standard (ETH, USB, HDMI, CAN, SPI, Camera, …)
  • 2 Gigabit Ethernet interfaces
• Computation of Non Player Character (NPC) behavior in Minecraft
• FPGA-based neural network implementation for AI acceleration
• >100x performance improvement
Benchmarking DNA Sequence Alignment

- CPU: Single-treaded implementation in C++
- GPU: Implementation using CUDA
- FPGA: Implementation using High Level Synthesis
Modular Microserver
Data Centre
M2DC Concept

• **Flexible and scalable architecture**

• **Low power microserver nodes (ARMv8)**

• **Built-in acceleration** (incl. FPGA-based microservers)

• **Intelligent power management**

• **Built-in enhancements** for performance, efficiency and security

• **Easy to integrate with data centre ecosystems**

• **Tailored to specific real-life applications**
**M2DC Appliances**

- **Photo processing**
  - Scalable photo finishing for leading online photo service

- **Cloud computing**
  - Enhanced IaaS, PaaS solutions exploiting heterogeneity

- **IoT data analytics**
  - Analysis of data from large numbers of sensors, e.g., for insurance companies

- **HPC**
  - Efficient meteorological simulations, used for predicting energy production
M2DC Server Architecture

• Architectural improvements focusing on communication
  • 10 GbE Network
  • PCIe switching
  • High-Speed Serial Communication
  • Scalable across rack level

• New Microservers
  • 64-bit ARM Server Processors / SoCs
  • Altera Stratix 10 SoC FPGAs
• iKVM/IPMI to every microserver, including fine-grained, high-speed monitoring
M2DC Server Architecture
Communication infrastructure

- 1/10 Gbit Ethernet management
- 10/40 Gbit Ethernet compute

Baseboard

Microserver Module

CPU  Mem  I/O

Microserver Module

CPU  Mem  I/O

Microserver Module

CPU  Mem  I/O

3/16 Microservers per Baseboard

Distributed Monitoring and KVM

GbE Switch

Compute Network Switch

Distributed Monitoring and KVM

GbE Switch

Compute Network Switch

Backplane

Up to 15 Baseboards per Server
• > 50 Gbit, low latency communication infrastructure
• Possibility to integrate storage and PCIe-based extension cards
Summary

FiPS – Field Programmable Servers

• RECS – Resource Efficient Cluster Server
  • Integration of CPUs, embedded/mobile CPUs, GPGPUs and FPGAs
• Evaluation using DNA sequencing
  • HLS FPGA implementation provides maximum energy efficiency

M2DC – Modular Microserver Data Centre

• Architectural improvements focusing on communication
• New Microservers (64-bit ARM, Stratix 10 SoC)
• Large scale testbeds / applications
Many Thanks!

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