Towards Next Generation Embedded Systems: Utilizing Parallelism and Reconfigurability

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Extended Abstract

This project envisions that the diversity of applications and contrasting performance constraints in next-generation embedded systems will necessitate the use of emerging technologies such as reconfigurable architectures and many-core processors. The project aims to develop, experiment and evaluate advanced embedded computing platforms for diverse application needs such as real-time response, low energy consumption and low cost constraints. Our focus is to address these needs through simplified programming and flexible architectures. This approach will provide the industry with tools and methodologies for meeting user-defined performance constraints with a quick time-to-market.

The project aims at exploring the potential of emerging computing platforms for enhanced performance in embedded systems. This approach will be supported through the use of a collection of architectural techniques that build on the essence of parallel program execution that are simple and easy to use. We are interested in exploring hardware platforms consisting of embedded microprocessors coupled with the state-of-the-art FPGAs and many-core processors. In developing the software methodology, our focus is on abstracting away low-level details of the underlying architecture, while supporting explicit mechanisms to allow portability and seamless task migration across heterogeneous devices. Overall, this scheme involves architectural design space exploration using of high-level programming and cross-layer modeling of the dataflow, hardware/software co-design for heterogeneity, and the support for dynamic run-time scheduling and tasks migration.

An international consortium that encompasses six partners is involved in the project: two academic (Amrita University and Halmstad University), three industrial (Texas Instruments, Maxim Integrated, Adarate) and one research institute (Swedish Defence Research Agency - FOI). In order to achieve the objectives of the project the consortium has been subdivided into constellations in accordance with the expertise and the contributions of the individual partner as follows:

1. HH, FOI, TIB, and MAX will work together to draw the functional requirements and specifications for the application development methodologies and framework. They will undertake the task to set up an assessment methodology for evaluation of the developed tools and frameworks. Examples of measures can be engineering efficiency or program portability.
2. AMU, ADS, TIB, FOI, and MAX will define the specifications for the target hardware architecture that could then be customized for the three use-cases considered in the project.
3. HH and AMU will co-develop the runtime system software required for monitoring, scheduling and distribution of tasks onto the hardware resources available in the target platform.