Heterogeneous Multi-Core Platform for Software-Defined Radio

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In the race for embedded computing power, homogeneous and heterogeneous approaches have been widely explored. Homogeneous processor arrays are easier to program using high-level languages and more or less automated development tools, but they generally cannot achieve high performance and low power consumption at the same time. An example on a homogeneous array of RISC processors is the Ninesilica platform developed at TUT [1,2]. In contrary, the heterogeneous solutions exploit specialized processors such as DSP, GPU, or Application-Specific Instruction-set Processors (ASIP) in addition to the general purpose processing, and/or accelerate processing with fixed or reconfigurable hardware blocks. One of the challenges in the heterogeneous systems is the diversity of programming interfaces and computing models.

Coarse-Grained Reconfigurable Arrays (CGRA) offer one alternative for accelerating embedded computing. They share the flexibility with FPGAs, but are a lot faster to be reconfigured and are operating on word-level computations and are thus better compatible with general-purpose programmable processors. On the other hand, they are very powerful as they utilize the hardware parallelism more efficiently than processors do. Examples of coarse-grained arrays from academia and industry are ADRES [3], PACT XPP [4], MORPHEUS [5], BUTTER [6] and CREMA [7].

Recently, a phenomenon known as Dark Silicon has been discovered, referring to the inability to operate the entire chip at its maximum clock frequency or even keep it clocked at all, due to extensive power density in modern silicon technologies [8]. It is shown that only 7% of 300mm^2 die can be used at full frequency within a power budget of 80W [9]. It turns out that CGRA is inherently solving this issue at least partially as it spreads the active computation sufficiently in space and time compared to centralized processing in a high clock-rate CPU. The prototype of a heterogeneous reconfigurable accelerator-rich multicore platform (HARP) [10] was designed to study how to tackle the Dark Silicon issues with heterogeneity. HARP is made up of one or a few general-purpose CPUs that are used to control a set of application-optimized CGRA blocks, see Fig. 1 [11]. The processor(s) can also run less intensive parts of the application software, whereas the most intensive kernels are implemented on reconfigurable hardware blocks. All the computing elements are connected by a Network-on-Chip.

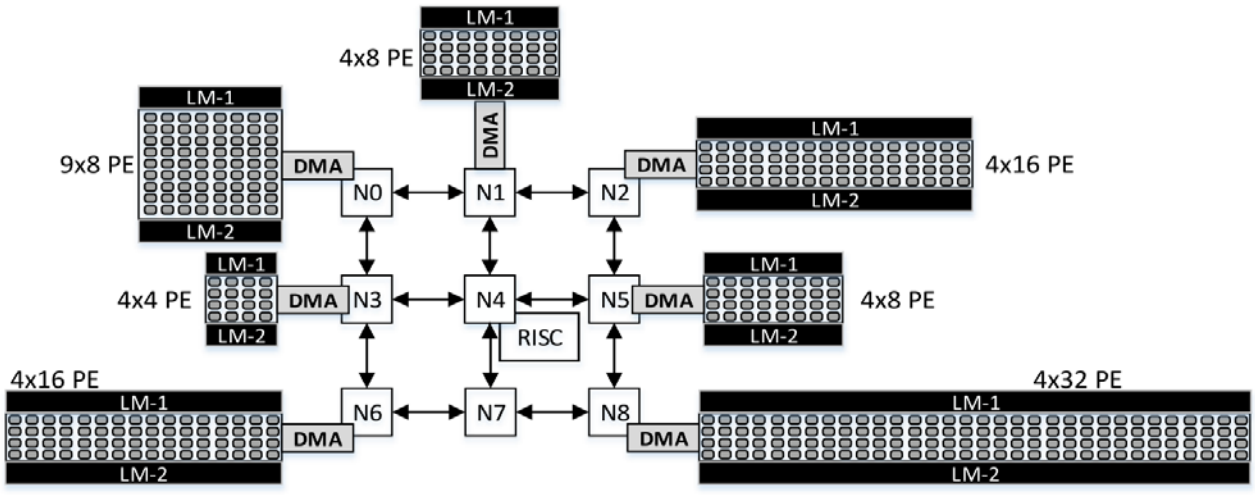

Fig. 1. An exemplary instance of the HARP platform.

The main application area of HARP is Software-Defined Radio (SDR) [12] which refers to flexible functionality based on programmable and/or reconfigurable implementation technologies. A review of SDR computing platforms can be found in [13], and the topic will be more thoroughly handled in an upcoming book [14]. HARP has turned out to be well-suited for SDR implementation. This talk will present the baseline CGRA architectures, the heterogeneous HARP platform, and will show examples on SDR style wireless communication implementations on the HARP blocks, such as FFT/IFFT, OFDM symbol synchronization, and channel equalizer for a WiFi receiver [15]. Preliminary performance and power efficiency results based on an FPGA prototype will also be discussed. Also, e.g., power mitigation by performance equalization is shown to be a viable technique for avoiding excess power consumption [16].

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