AXIOM: enabling parallel processing in cyber-physical systems

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***Abstract*—The AXIOM project focuses on developing an affordable CPS node that features general purpose capability coupled with reconfigurable resources. The nodes will be interconnected and a programming layer will turn them into a parallel processing system. The programming layer also makes easier the use of the reconfigurable resources for accelerators. Harnessing the combined CPS resources enables a new level of "edge" processing. We will focus on the interconnection and modularity aspects of the project, and present the current status and the challenges we are facing mainly in performance and efficiency.**

***Keywords*-Cyber-Physical Systems, Parallel Programming Models, High-speed interconnect**

I. Introduction

The AXIOM project (Agile, eXtensible, fast I/O Module) aims at researching new software/hardware architectures for the future Cyber-Physical Systems (CPSs) [1], [2]. More specifically, AXIOM targets:

- Realizing a small board that is flexible, energy efficient and modularly scalable, by utilizing the latest Xilinx Zynq platforms with custom high-speed interconnects to build the AXIOM prototype board.
- Fast and easy programmability of multi-core, multi-board, FPGA node, with the OmpSs programming model [3] that provides improved thread management and real-time support from the operating system.
- Seamless interfacing with the Cyber-Physical world, based on the popular Arduino shields [4] that will be pluggable onto the board.
- ontribute to standards, in the context of the Standardization Group for Embedded Systems (SGET) and OpenMP.

Within this paper, we focus on the interconnection and modularity aspects of the project, and present the current status and the challenges we are facing mainly in performance and efficiency: Section II describes the AXIOM high-speed interconnect, and Section III a first set of preliminary results. Finally Section IV concludes the paper.

II. The AXIOM High-speed interconnect

FPGAs are considered the most energy efficient approach for specific tasks [5]. Within the AXIOM project, the choice is toward chips from the Xilinx Zynq MPSoC family that include ARM® processors, integrate UltraRAM modules, high-speed transceivers, low-power programmable logic, DSP slices, PCI express, DDR3 memory controller, and other peripherals such as USB, Gbe, etc. The main focus for the FPGA is to become the "central heart" of the board making possible to integrate these features, and also provide customized and reconfigurable acceleration of the specific scenario where the board is deployed, providing the necessary substrate for board-to-board communication.

AXIOM-based systems will target "mid-range" high performance computing by utilizing reconfigurable SoCs, interconnected using high-speed serial transceivers. The communication layer is the backbone of any distributed system, and if not carefully designed and implemented can lead to network congestion, low throughput, high latency and poor overall system performance. For this reason, the AXIOM interconnect is designed with two key-parameters in mind, (a) high-performance to meet application demands, and (b) low resource utilization, so it can be implemented even to small-ranged reconfigurable SoCs.

The AXIOM interconnect provides a network interface (NI) that supports remote direct memory access (RDMA) transactions (reads and writes), as well as direct transmission of raw data and control messages. At the same time, it is based on a low OS intrusive approach using a minimal set of interrupts, hence introducing minimal performance overheads. The AXIOM interconnect supports demanding applications with high-throughput, and at the same time targets processing platforms that are bundled with minimal reconfigurable resources.

The AXIOM platform is designed based on Xilinx Zynq devices that feature a dual- or quad-core ARM Cortex A9 processor, tightly coupled with FPGA fabric. The high-speed interconnect will utilize the integrated gigabit-rate transceivers with relatively low-cost USB-C connectors to

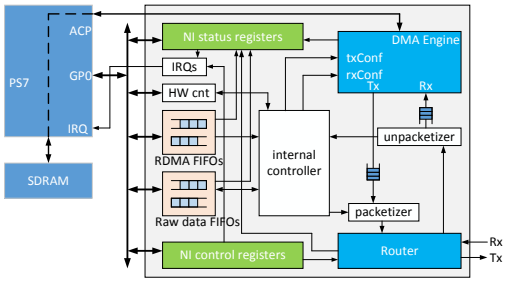

Figure 1: The AXIOM network interface architecture.

interconnect multiple boards. Such connectivity will allow to build (or upgrade at a later moment) flexible and low-cost systems by cascading more AXIOM boards, without the need of costly connectors and cables. AXIOM boards will feature two or four bi-directional links, so that the nodes can be connected in many different ways, such as ring and 2D-mesh/torus.

The integrated processing system (PS7) of each board, communicates using an on-chip network interface (NI) - implemented in the FPGA region- that efficiently supports the application communication protocols. Figure 1 illustrates the NI architecture, which implements remote direct memory access (RDMA) and remote-write operations as basic communication primitives visible at the application level.

The AXIOM NI, shown in Figure 1, supports (a) RDMA read and write transactions, in order to enhance the performance of applications that require large memory regions, and (b) raw data and control messages exchange for minimal network control overheads. At the same time, it will follow a minimal CPU intervention approach, as it supports a minimal set of interrupts to signal a HW state change (e.g. a physical link is down), and also directly manages all local and remote ACKs. On the implementation perspective, in order to provide a high-performance interconnect module among all processing nodes, the AXIOM NI will provide on-chip message queues, where the OS posts message descriptors and gets updates of finished transactions, such as RDMA reads and writes.

III. Preliminary Results

In our initial set of experiments, we performed a first evaluation of the DMA engine and the physical network interconnect medium; we connected the processing system (PS7) to a DMA engine, and the latter using the AXI stream protocol with the Aurora IP. In our current configuration, the Aurora IP utilizes only one MGT transceiver. We mapped the same experimental system on two ZC706 FPGA boards, connected with SMA cables; the design occupied 10583 (4.8%) LUTs, 12452 FFs (2.8%), and 5 BRAMs (0.9%) Zynq 7045 SoC. The Aurora IP configuration generated the user clock at 156.25 MHz that was used to also clock the DMA engine.

Table I: Tests run on Linux 14.04 Linaro distribution (throughput in MB/sec).

Data size (MB)	Round-trip w copy	Round-trip w/o copy	Single-trip
0.5	16.05	146.77	293.25
1.0	16.06	147.31	294.58
2.0	16.06	147.58	295.18
4.0	16.06	147.71	295.47

We ran a set of experiments on the PS7 for single and round-trip data transmissions between the two boards, ranging from 0.5 to 4 MB using a Linux 14.04 Linaro-based configuration (Table I). The "Round-trip w copy" test copies received data to another memory location before they are relayed back to the original sender, whereas the "Round-trip w/o copy" omits the intermediate data copy. As observed, the Linux-based implementation can reach up to $\tilde{3}$00 MB/sec or 2400 Gbits/sec. Consequently, a 4-MGT interconnection could reach up to 9.6 Gbits/sec.

IV. Conclusions and Future Work

In this paper, we presented the AXIOM high-speed interconnect architecture. Based on the first set of our preliminary results, we can see that the AXIOM interconnect does offer high-performance and at the same time low resource utilization, making realizable even to small-ranged reconfigurable SoCs. Our next steps are (a) migrating our current system to the Ultrascale+ SoC, and (b) the final NI and router integration to the AXIOM platform.

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